IN THE CLAIMS

1. (Currently Amended) A semiconductor device for refreshing data stored in a memory device, comprising:

a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells wherein the N number of unit cell blocks are corresponded to logical cell block addresses and one unit cell block is added for accessing data with high speed;

a tag block having N+1 number of unit tag blocks, each unit tag block storing at least one physical cell block address ~~denoting a row address~~ storing ~~a~~ data wherein the tag block receives a logical cell block address designated for accessing one of N number of unit cell blocks and converts the logical cell block address into a physical cell block address designated for accessing one of the N+1 number of unit cell blocks; and

a control means for controlling the tag block and ~~the~~ a predetermined cell block table for refreshing the data in the plurality of unit cells coupled to a word line in response to the at least one physical cell block address

wherein the tag block stores information representing the converted physical cell block address and a refresh operation is preformed through the use of the information.

2. (Currently Amended) The semiconductor device as recited in claim 1, further comprising:

a predetermined cell block table for storing ~~an~~ information representing at least more than one word line among the M number of the word lines storing data.

3. (Currently Amended) The semiconductor memory device as recited in claim 1, wherein the tag block includes:

an N+1 number of unit tag tables corresponded to the N+1 unit cell blocks, each unit tag table having M number of registers for storing the at least one physical cell block address denoting a row address storing ~~a~~ data;

a N+1 number of comparators corresponded to the N+1 number of unit tag, each

comparator for ~~checking~~ comparing address information stored in ~~the~~ registers of the corresponding unit tag table ~~for comparing selected one word line of selected unit cell block~~ with a logical cell block address sensed by the row address wherein the address information is the at least one physical cell block address denoting the row address storing the data;

a encoder for outputting the at least one physical cell block address by encoding results compared by the N+1 number of comparators; and

a tag control block for controlling the N+1 number of the unit tag tables, the N+1 number of the comparators, and the encoder.

4. (Currently Amended) The semiconductor memory device as recited in claim 3, wherein each register of ~~the~~ a unit tag table includes:

a first register having X bits for storing the logical cell block address ~~in response to the N number of unit cell blocks~~ representing a unit cell block, wherein X is at least $\log_2 N$; and

a second register for ~~sensing~~ storing the information representing an update of data stored in the first register.

5. (Currently Amended) The semiconductor memory device as recited in claim 3, wherein the tag block further includes:

a decoder for receiving ~~the~~ candidate information and outputting the logical cell block address.

6. (Currently Amended) The semiconductor memory device as recited in claim ~~2~~ 4, wherein the predetermined cell block table includes M number of third registers for storing information ~~what unit cell block out of~~ which word lines of (N+1) * M word lines included in the N+1 number of the physical unit cell blocks ~~has~~ are the M number of the predetermined word lines, each third register having X+1 bits.

7. (Currently Amended) A method for a refresh operation of a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a tag block having N+1

number of unit tag blocks, each having M number of registers for sensing an update of data, comprising the steps of:

(A) starting a refresh mode in response to a refresh signal;

(B) finding at least one physical cell block address and word line determined by the physical cell block address having data by ~~decoding~~ checking $(N+1)\times M$ number of ~~second~~ registers in the tag block, each register storing a logical block address and an information representing an update of the logical block address ; and

(C) performing the refresh operation ~~in the selected unit cell block~~ through the use of the information,

wherein the N number of unit cell blocks are corresponded to addresses and one unit cell block is added for accessing data with high speed.

8. (Currently Amended) The method as recited in claim 7, wherein the step (C) includes the step of

(D) ~~decoding~~ denoting ~~the~~ M number of ~~third~~ registers in ~~the~~ a predetermined cell block table in order to find out ~~that the~~ an address representing M number of predetermined word lines ~~is respectively~~ assigned ~~to which unit cell block~~ among (N+1) * M word lines of the N+1 number of unit cell blocks,

wherein the refresh operation is performed except for ~~word lines assigned as~~ the address representing the M number of the predetermined word lines.